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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
YOR920030488US1 (163-16)

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Application Number	Filed
10/715,225	November 17, 2003

First Named Inventor
Arun Kwangil Iyenar

Art Unit	Examiner
2186	Sheng Jen Tsai

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☑ attorney or agent of record. Registration number 43,584

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

Signature

Frank V. DeRosa
Typed or printed name

516-496-3868
Telephone number

17 April 2008
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.
Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 1 forms are submitted.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Iyengar et al.	**Examiner: Sheng Jen Tsai**
Serial No: 10/715,225	**Group Art Unit: 2186**
Filed: November 17, 2003	**Docket: YOR920030488US1 (163-16)**

For: SYSTEM AND METHOD FOR ACHIEVING STRONG DATA CONSISTENCY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Statement in Support of Pre-Appeal Brief Request for Review

This paper is being filed in support of Applicants' Pre-Appeal Brief Request for Review. A Notice of Appeal has been filed herewith in response to the Final Office Action mailed on 17 January 2008. Applicants respectfully contend that the claim rejections set forth in the Final Office Action are clearly erroneous as a matter of fact and law for at least those reasons set forth in the After Final Response filed on 17 March 2008, which is incorporated herein by reference. Rather than reiterate those reasons in full, the following Statement will focus on the impropriety of the Examiner's obviousness rejection of independent claims 1, 10, 11, 17 and 18 based on Iyengar and Hiraoka.

Applicants respectfully assert that claims 1, 10, 11, 17 and 18 include features that are clearly not disclosed or suggested by Iyengar and Hiraoka, either singularly or in combination. More importantly, the Examiner's obviousness analysis is factually and legally flawed and based on unfounded interpretations of the claims as applied to the teachings of the cited references.

In general, the claimed inventions (claims 1, 10, 11, 17 and 18) are directed to systems and methods for managing objects to ensure cache consistency/coherency in a shared memory system where a plurality of caches may store a local copy of an object. A cache consistency coordinator is provided to receive *object update commands*, send instructions to those storage elements that are deemed to store a copy of the object (to be

updated) to invalidate their local copy of the object, *wherein the updating of the object is delayed until the consistency coordinator determines that each storage element instructed to invalidate a copy of the object either (i) has acknowledged that it is not storing a valid copy of the objector or (ii) is unresponsive.*

In formulating the rejections, the Examiner seemingly relies on Iyengar as generally disclosing that a central cache may communicate with local caches to make sure that copies of an object to be updated are invalidated. However, Iyengar does not specifically teach that updating of the object is *delayed until it is determined that each storage element instructed to invalidate a copy of the object has either (i) acknowledged that it is not storing a valid copy of the object or (ii) been deemed unresponsive,* as recited in the claimed inventions. In fact, the Examiner acknowledges at the very least that Iyengar does not specifically disclose *delaying an updating of the object until it is determined that each storage element instructed to invalidate a copy of the object has . . . been deemed unresponsive.*

However, the Examiner seemingly relies on the teachings of Hiraoka in Col. 4, lines 41-50 as curing the deficiencies of Iyengar in this regard. But it is respectfully submitted that the Examiner's reliance on Hiraoka is wholly misplaced in this regard, as Hiraoka does not fairly teach or suggest *delaying an updating of the object until it is determined that each storage element instructed to invalidate a copy of the object has . . . been deemed unresponsive.*

In the Advisory Action, the Examiner notes that with regard to the claimed feature of *delaying an updating of the object until it is determined (by the consistency coordinator) that each storage element instructed to invalidate a copy of the object has either (i) acknowledged that it is not storing a valid copy of the object or (ii) been deemed unresponsive,* the "core event" is "to invalidate a copy of the object. The Examiner further notes that the process by Hiraoka to purge a local copy of the TLB (table look aside buffer) is the same as "to invalidate a copy of the object." Indeed, the Examiner further notes in the Advisory Action that "a TLB certainly qualifies as an object and the purging the TLB would actually invalidate the TLB.

These arguments are *too* simplistic and are made out of context and with no due consideration of scope of the claimed inventions, as a whole. This can be readily seen by replacing the claim term "object" with TLB as follows: *delaying an updating of the* **TLB** *until it is determined that each storage element instructed to invalidate a copy of the* **TLB** *has either (i) acknowledged that it is not storing a valid copy of the* **TLB** *or (ii) been deemed unresponsive.*

This interpretation makes no sense on various levels. First of all, it is well known that a TLB (translation look aside buffer) is a cache of PTEs (page table entries), which is used by memory management hardware to improve the speed of virtual address translation. In general, most, if not all, state of the art processor technologies use a TLB, wherein a TLB has a fixed number of slots containing page table entries, which map virtual addresses onto physical addresses. In this regard, the Examiner's contention that the TLB is "certainly an object" that is stored in a cache is not factually correct, as the TLB is a cache structure that stores page table entries. In this regard, initializing or pursing a TLB is a process that involves purging the page table entries stored in the TLB cache structure.

Another fundamental flaw in the Examiner's analysis is that a "core event" (of the claimed process step in issue) is not *invalidating a copy of the object* as suggested by the Examiner, but rather *delaying an updating of the object* until certain events/conditions occur. In this regard, the Examiner's reliance on Hiraoka is misplaced. Even assuming that the **TLB** is a cached "object," there is nothing in Hiraoka that suggests *delaying an updating of the* **TLB** *until it is determined that each storage element instructed to invalidate a copy of the* **TLB** *has either (i) acknowledged that it is not storing a valid copy of the* **TLB** *or (ii) been deemed unresponsive*

The Examiner states (in the Advisory Action) that in Hiraoka, the "*source processor delays the updating* ... ", but the Examiner fails to explain how or where or what "updating a TLB" refers to in the context of the Hiraoka process. Indeed, even assuming, *arguendo*, that "purging" (initializing) a TLB can be deemed to be "invalidating a local copy of an object", in the proper context of the claimed invention,

the Examiner simply ignores and fails to explain what would constitute "updating the TLB" in the Hiraoka system.

However, Hiraoka teaches that in a virtual memory control multiprocessor system, the purging (initialization) of TLBs of all process must be performed to equalize the contents of the TLBs (see Col. 1, lines 10-15). Hiraoka is merely directed to a system for purging the contents of TLB (table look aside butters) of a set of parallel processors. The teachings of Hiraoka regarding the process for purging TLBs of a multiprocessor system are very much different and irrelevant to the systems and methods as contemplated by the claimed inventions for maintaining consistency of copies of an object stored in storage elements.

In fact, as noted above, Hiraoka teaches that initialization (purging) of all processors must be completed at certain times for all processors. In this regard, there is nothing in Hiraoka that fairly teaches or suggests that the purging of one of the processors in a multiprocessor system can be skipped or disregarded (and subsequent tasks performed) in the event of a timeout condition (after issuance of a purge request signal) if one processor is unresponsive.

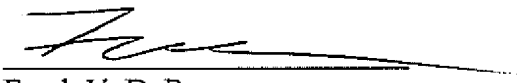
The Examiner relies on Col. 4, lines 41-50 of Hiraoka as teaching delaying updating until a processor is deemed unresponsive. However, Hiraoka teaches in Col. 4, lines 41-50 the following:

> The above operation can be performed when all the processors 20_0 through 20_3 are present. However, when the processor 20_3 is not present, the following operation is performed. The signal 48_3 representing that the processor 20_3 is not present is set at logic "1". The signal 48_3 of logic "1" is supplied to the OR gate 42_3. The OR gate 42_3 supplies the dummy TLB purge end signal to the AND gate 43. If the processor 20_3 is not present, the processor 20_0 can detect that all the TLB purge operations of the processors 20_0 through 20_2 are completed.

There is nothing in the cited paragraph relating to an unresponsive processor, but merely a condition in which the multiprocessor system comprise 3 processors instead of 4. As such, it is respectfully submitted that the Examiner's reliance on the cited passage is clearly misplaced.

In view of the above, claims 1, 10, 11, 17 and 18 include features that are not disclosed or suggested by Iyengar and Hiraoka, either singularly or in combination, and are thus, non-obvious over such combination. Given that all remaining obviousness rejections for those claims depending from independent claims 1, 10, 11, 17 and 18 are based directly or primarily on the combination of Iyengar and Hiraoka as applied to the independent claims, all obviousness rejections are legally deficient for at least the same reasons given above. Accordingly, withdrawal of the obviousness rejections is respectfully requested.

Respectfully submitted,



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